IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
David J. HATHAWAY et al.
Serial No.: 10/709,362
Filed: April 29, 2004

Docket No. P27064
Confirmation No. 3361
Group Art Unit: No. 2863
Examiner: T. M. Le

For: **SYSTEM AND METHOD OF ANALYZING TIMING EFFECTS OF SPATIAL DISTRIBUTION IN CIRCUITS**

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

AMENDMENT UNDER 37 C.F.R. §1.112

Sir:

In response to the non-final Office Action dated December 23, 2005, please amend the above-identified application as follows.

Amendment to the claims are set forth on pages 2-9.

Remarks are set forth on pages 10.

If extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. §1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to Deposit Account No. 09-0456.

AMENDMENT TO THE CLAIMS

Please **AMEND** claims 1 and 14; and

Please **ADD** claim 31 as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A method for analyzing the timing of a circuit, comprising:

determining at least one location information for one or more inputs to a timing test; and

computing a timing slack variation for the timing test using the at least one location information,

wherein the one or more inputs comprise cells or elements of interest, and

wherein the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

2. (Original) The method of claim 1, wherein the input to a timing test is a path or a logic cone.

3. (Original) The method of claim 1, wherein the at least one location information comprises a bounding region for the one or more inputs to the timing test.

4. (Original) The method of claim 3, wherein said determining comprises defining the bounding region based on the locations of the one or more inputs to the timing test.

5. (Original) The method of claim 4, wherein said determining further comprises modifying a size of the bounding region to account for variations in delay among the one or more inputs to the timing test.

6. (Original) The method of claim 5, wherein said computing comprises:

determining a slack variation factor based on the size of the bounding region; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

7. (Previously Presented) A method for analyzing the timing of a circuit, comprising:

determining at least one location information for one or more inputs to a timing test; and

computing a timing slack for the timing test using the at least one location information,

wherein the at least one location information comprises a centroid of the one or more inputs to the timing test.

8. (Original) The method of claim 7, wherein the centroid comprises the averaged location of the one or more inputs to the timing test.

9. (Original) The method of claim 7, wherein the centroid comprises the delay-weighted averaged location of the one or more inputs to the timing test.

10. (Original) The method of claim 7, wherein said determining comprises:

calculating a first centroid of a first input to the timing test;

calculating a second centroid of a second input to the timing test; and

determining the distance between the first and second centroids.

11. (Original) The method of claim 10, wherein said calculating comprises:

determining a slack variation factor based on the distance between the first and second centroids; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

12. (Original) The method of claim 1, wherein the at least one location information comprises an abstract location information.

13. (Original) The method of claim 12, wherein the abstract location information is based upon correlation of delay functions.

14. (Currently Amended) A computer-readable medium containing instructions that, when executed, cause a computer to:

determine at least one location information for one or more inputs to a timing test; and

compute a timing slack variation for the timing test using the at least one location information,

wherein the one or more inputs comprise cells or elements of interest, and

wherein the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

15. (Original) The medium of claim 14, wherein the input to a timing test is a path or a logic cone.

16. (Original) The medium of claim 14, wherein the at least one location information comprises a bounding region for the one or more inputs to the timing test.

17. (Original) The medium of claim 16, wherein said determining comprises defining the bounding region based on the locations of the one or more inputs to the timing test.

18. (Original) The medium of claim 17, wherein said determining further comprises modifying a size of the bounding region to account for variations in delay among the one or more inputs to the timing test.

19. (Original) The medium of claim 18, wherein said computing comprises:

determining a slack variation factor based on the size of the bounding region; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

20. (Previously Presented) A computer-readable medium containing instructions that, when executed, cause a computer to:

determine at least one location information for one or more inputs to a timing test; and

compute a timing slack for the timing test using the at least one location information,

wherein the at least one location information comprises a centroid of the one or more inputs to the timing test.

21. (Original) The medium of claim 20, wherein the centroid comprises the averaged location of the one or more inputs to the timing test.

22. (Original) The medium of claim 20, wherein the centroid comprises the delay-weighted averaged location of the one or more inputs to the timing test.

23. (Original) The medium of claim 20, wherein said determining comprises:

calculating a first centroid of a first input to the timing test;

calculating a second centroid of a second input to the timing test; and

determining the distance between the first and second centroids.

24. (Original) The medium of claim 23, wherein said computing comprises:

determining a slack variation factor based on the distance between the first and second centroids; and

adding the slack variation factor to a timing slack calculated for the one or more inputs to the timing test.

25. (Original) The medium of claim 14, wherein the at least one location information comprises an abstract location information.

26. (Original) The medium of claim 25, wherein the abstract location information is based upon correlation of delay functions.

27. (Original) A method of analyzing the timing of an integrated circuit, comprising:

identifying an early path and a late path in the integrated circuit;

determining a timing slack variation in the early path using location information on one or more elements in the early path;

determining a timing slack variation in the late path using location information on one or more elements in the late path; and

computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path.

28. (Original) The method of claim 27, wherein the location information on the one or more elements in the early path and the location information on the one or more elements in the late path comprise bounding regions defined around the one or more elements in the early path and the one or more elements in the late path, respectively.

29. (Original) The method of claim 27, wherein the location information on the one or more elements in the early path and the location information on the one or more elements in the late path comprise centroids calculated by considering the one or more elements in the early path and the one or more elements in the late path, respectively, as aggregates.

30. (Original) The method of claim 27, wherein the method is performed for an early mode timing analysis of the integrated circuit and a late mode timing analysis of the integrated circuit.

31. (New) The medium of claim 20, wherein a delay in circuit paths is predicted by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

REMARKS

Claims 1-31 are currently pending in the application. By this amendment, claims 1 and 14 are amended and claim 31 is added. The above amendments and added claim does not add new matter to the application and are fully supported by the specification. For example, support for the amendment to claims 1 and 14, and new claim 31 can be found at paragraphs [0018] of the instant published US patent application 2005/02466117. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Allowable Claims

Applicants appreciate the indication that claims 10, 11, 23 and 24 contain allowable subject matter. These claims are not being presented in independent form at this time because claims 7 and 20, from which these claims depend, are believed to be allowable. Furthermore, Applicants submit that all of the pending claims are in condition for allowance and that the rejection under § 102 should be withdrawn.

35 U.S.C. § 102(a) Rejection

Claims 1-9, 12-22 and 25-30 were rejected under 35 U.S.C. § 102(a) as being anticipated by the Article entitled "Block-based Static Timing Analysis with Uncertainty" by Anirudh DEVGAN et al. This rejection is respectfully traversed.

In order to establish a *prima facie* case of anticipation under 35 U.S.C. § 102, a single prior art reference must disclose each and every element as set forth in the subject claim. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2

USPQ 2d 1051, 1053 (Fed. Cir. 1987). Applicants respectfully submit that a *prima facie* case of anticipation has not been established as the applied reference fails to teach each and every element of the claims.

More particularly, independent claims 1 and 14 recite, *inter alia,*

> wherein the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution.

Additionally, independent claims 7 and 20 recites, *inter alia,*

> computing a timing slack for the timing test using the at least one location information, wherein the at least one location information comprises a centroid of the one or more inputs to the timing test.

Furthermore, independent claim 27 recites, *inter alia,*

> determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and, computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path.

The applied reference does not teach, or even suggest, at least these features.

Applicants acknowledge that DEVGAN discloses a statistical timing analysis wherein "delay and arrival times in the circuit are modeled and as random variables" (see page 608 col. 1, lines 19-21). Applicants also acknowledge that DEVGAN discloses that "critical paths and slack distributions can be computed for a given probability or confidence level" (see page 608, col. 2, lines 9-23). However, it is not apparent that DEVGAN discloses, or even suggests, that the method predicts a delay in circuit paths by considering a portion of the delay that is influenced by a proximity of circuit elements in a path or paths separately from a full delay distribution (claims 1 and

14). Applicants note, in particular, that the Examiner has failed to identify any disclosure in this document indicating that the disclosed analysis even accounts for a proximity of circuit elements in a path or paths, much less, doing so separately from a full delay distribution.

Furthermore, while the Examiner has identified page 610, col. 1, lines 6-17 and pages 610-612, section 3 and Fig. 9 as disclosing that the at least one location information comprises a centroid of the one or more inputs to the timing test (claims 7 and 20), it is apparent that the cited language is silent with regard to utilizing in the analysis a centroid of the one or more inputs to the timing test. Nor has the Examiner explained how such language or the drawing of Fig. 9 can be interpreted to disclose or suggest utilizing a centroid of the one or more inputs to the timing test in the analysis.

Moreover, while the Examiner has alleged that DEVGAN discloses determining a timing slack variation in the early path using location information on one or more elements in the early path, determining a timing slack variation in the late path using location information on one or more elements in the late path, and computing a new timing slack for the early path and the late path by using the timing slack variation in the early path and the timing slack variation in the late path at pages 608-610, the Examiner has failed to identify any specific language in this document in support of such assertions. Applicants note, for example, that while the noted language discusses comparing deterministic arrival times and probabilities thereof (see Fig. 3), there is no apparent disclosure or suggestion indicating that both early and late paths are accounted for, much less, that a timing slack variation thereof is utilized in the analysis.

Nor has the Examiner explained how the noted language can be interpreted to disclose or suggest these features.

Applicants emphasize that whereas DEVGAN uses a statistical probability analysis to determine critical paths and slack distributions, the invention, by way of example, uses actual determined information in the timing test.

Furthermore, dependent claims 2-6, 12, 13, 15-19, 25, 26, 28 and 30 recite additional features which are not disclosed, or even suggested, by DEVGAN and the Examiner has not shown otherwise.

For example, DEVGAN clearly fails to disclose the logic cone of claims 2 and 15, the bounding region recited in claims 3-6, 16-19 and 28, and the abstract location information of claims 12, 13, 25 and 26. In particular, whereas DEVGAN teaches determining the information statistically for paths, it is not correct that DEVGAN teaches gathering one set of information for the entire input cone.

Accordingly, Applicants respectfully submit that the rejection under 35 U.S.C. § 102(a) should be withdrawn.

Comments on Reasons for Allowance

In response to the Statement of Reasons for Allowance set forth in the Office Action, Applicants wish to clarify the record with respect to the basis for the patentability of the indicated claims in the present application. In this regard, while Applicants do not disagree with the Examiner's indication that certain identified features are not disclosed by the references, Applicants submit that the claims in the present application recite a

combination of features, and that the basis for patentability of these claims is based on the totality of the recited features.

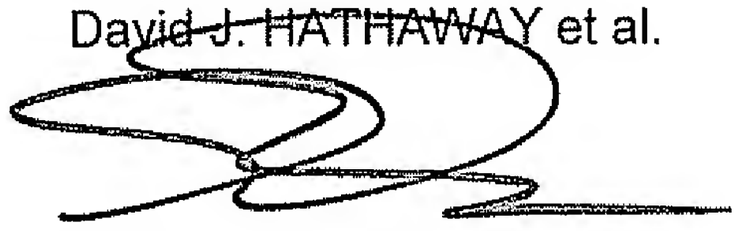
New Claims are also Allowable

Applicants submit that the new claim 31 is allowable over the applied art of record. Specifically, claim 31 depends from claim 20 which are believed to be allowable. Additionally, claim 31 recites a combination of features which are clearly not disclosed or suggested by the applied art of record. Accordingly, Applicants respectfully request consideration of these claims and further request that the above-noted claims be indicated as being allowable.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants hereby make a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0456.

Respectfully submitted,
David J. HATHAWAY et al.



Andrew M. Calderon
Registration No. 38,093

March 15, 2006
Greenblum & Bernstein, P.L.C.
1950 Roland Clarke Place
Reston, Virginia 20191
Telephone: 703-716-1191
Facsimile: 703-716-1180